Amendments to the Specification :

Please replace paragraph [0012] with the following amended paragraph:

a1

[0012] The memory array 1 comprises a plurality of memory cells 11 arranged in ~~a~~ rows 13 and columns 14. A row of memory cells includes first and second wordlines 103a-b. The first wordline is controlled by a first row decoder 21a and the second wordline is controlled by a second row decoder 21b. A column of memory cells includes first and second bitlines 101a-b. First sense amplifiers 107a are coupled to the first bitlines and second sense amplifiers 107b are coupled to the second bitlines.

Please replace paragraph [0018] with the following amended paragraph:

a2

[0018] Fig. 4 shows an operational diagram of a control circuit 4 in accordance with one embodiment of the invention. The control circuit, for example, is a state machine. The control circuit comprises a control block 61. The control block receives a system clock signal CLK which controls the function of the memory module. The IC can have two modes of operation, ~~poser~~ power down or normal. The operating modes of the IC can be controlled by the PD signal. In one embodiment, a second clock signal is provided to the control block. The second clock signal is generated by, for example, an oscillator 60.

Please replace paragraph [0022] with the following amended paragraph:

a3

[0022] State 2 represents the case where a memory access is requested through port ~~B~~ A while a refresh is requested. The addresses of the refresh and access are compared. If the addresses of the access and refresh are to different rows, the access is conducted through port ~~B~~ A while the refresh operation is allocated to port ~~A~~ B. The row corresponding to the refresh address is refreshed through port ~~A~~ B. Alternatively, a memory access through port B is requested simultaneously with a refresh request, as represented by state 3. In such a case, the memory access is performed through port B while the refresh is conducted through port A if the addresses of the access and refresh are to different rows.